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Japanese Patent Laid-Open Publication No. Heisei 9-8205

(TITLE OF THE INVENTION)

RESIN-ENCAPSULATED SEMICONDUCTOR DEVICE

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(CLAIMS)

1. A resin-encapsulated semiconductor device using a lead frame which is shaped in accordance with a two-step etching process to a body wherein a thickness of inner leads is less than that of the lead frame blank, comprising:

inner leads having the thickness less than that of the lead frame blank; and

terminal columns integrally connected to the inner leads and having the same thickness with the lead frame blank, the terminal columns possessing a column-shaped configuration which is adapted to be electrically connected to an external circuit, the terminal columns being disposed outside of the inner leads in a manner such that they are coupled to the inner leads in a direction orthogonal to the thickness-wise direction thereof, the terminal columns having terminal portions arranged on top ends thereof, the terminal portions being made of solders, etc. and exposed to the outside beyond a resin encapsulate, each inner lead possessing a rectangular cross-section and having four

surfaces including a first surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surface of a remaining portion of the inner lead having the same thickness with the lead frame blank while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

2. A resin-encapsulated semiconductor device using a lead frame which is shaped in accordance with a two-step etching process to a body wherein a thickness of inner leads is less than that of the lead frame blank, comprising:

inner leads having the thickness less than that of the lead frame blank; and terminal columns integrally connected to the inner leads and having the same thickness with the lead frame blank, the terminal columns possessing a column-shaped configuration which is adapted to be electrically connected to an external circuit, the terminal columns being disposed outside of the inner leads in a manner such that they are coupled to the inner leads in a direction orthogonal to the thickness-wise direction thereof, portions of top ends of the terminal columns being exposed to the outside beyond a resin encapsulate, each inner lead possessing a rectangular

cross-section and having four surfaces including a first surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surface of a remaining portion of the inner lead having the same thickness with the lead frame blank while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

10 3. The resin-encapsulated semiconductor device as claimed in claims 1 or 2, wherein a semiconductor chip is received inward of the inner leads, and electrodes of the semiconductor chip are electrically connected to the inner leads through wires, respectively.

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4. The resin-encapsulated semiconductor device as claimed in claim 3, wherein the lead frame has a die pad, and the semiconductor chip is mounted onto the die pad.

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5. The resin-encapsulated semiconductor device as claimed in claim 3, wherein the lead frame does not have a die pad, and the semiconductor chip is fastened to the inner leads using a reinforcing fastener tape.

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6. The resin-encapsulated semiconductor device as

claimed in claims 1 or 2, wherein the semiconductor chip is fastened by means of insulating adhesive to the second surfaces of the inner leads on one surface thereof on which the electrodes are located, and the electrodes of the semiconductor chip are electrically connected to the first surfaces of the inner leads through wires, respectively.

5 7. The resin-encapsulated semiconductor device as claimed in claims 1 or 2, wherein the semiconductor chip is fastened to the second surfaces of the inner leads by bumps thereby to be electrically connected to the inner leads.

(DETAILED DESCRIPTION OF THE INVENTION)

(FIELD OF THE INVENTION)

10 15 The present invention relates to a resin-encapsulated semiconductor device capable of meeting the requirement for an increase in the number of terminals and resolving problems which are caused in association with position shift and coplanarity of an outer lead.

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(DESCRIPTION OF THE PRIOR ART)

FIG. 15(a) shows the configuration of a generally known resin-encapsulated semiconductor device (a plastic lead frame package). The shown resin-encapsulated 25 semiconductor device includes a die pad 1511 having a

semiconductor chip 1520 mounted thereon, outer leads 1513 to be electrically connected to the associated circuits, inner leads 1512 formed integrally with the outer leads 1513, bonding wires 1530 for electrically connecting the tips of the inner leads 1512 to the bonding pad 1521 of the semiconductor chip 1520, and a resin 1540 encapsulating the semiconductor chip 1520 to protect the semiconductor chip 1520 from external stresses and contaminants. This resin-encapsulated semiconductor device, after mounting the semiconductor chip 1520 on the bonding pad 1521, is manufactured by encapsulating the semiconductor chip 1520 with the resin. In this resin-encapsulated semiconductor device, the number of the inner leads 1512 is equal to that of the bonding pads 1521 of the semiconductor chip 1520. And, FIG. 15(b) shows the configuration of a monolayer lead frame used as an assembly member of the resin-encapsulated semiconductor device shown in FIG. 15a. Such a lead frame includes the bonding pad 1521 for mounting the semiconductor chip, the inner leads 1512 to be electrically connected to the semiconductor chip, the outer lead 1513 which is integral with the inner leads 1512 and is to be electrically connected to the associated circuits. This also includes dam bars 1514 serving as a dam when encapsulating the semiconductor chip with the resin, and a frame 1515 serving to support the entire lead frame 1510.

Such a lead frame is formed from a highly conductive metal such as a cobalt, 42 alloy (a 42% Ni-Fe alloy), copper-based alloy by a pressing working process or an etching process. FIG. 15(b)(D) is a cross-sectional view taken along the 5 line F1-F2 of FIG. 15(b)(1).

Recently, there has been growing demand for the miniaturization and reduction in thickness of resin-encapsulated semiconductor device employing lead frames like the lead frame (plastic lead frame package) and the 10 increase of the number of terminals of resin-encapsulated semiconductor package as electronic apparatuses are miniaturized progressively and the degree of the integration of semiconductor device increase progressively. Thus, recent resin-encapsulated semiconductor package, 15 particularly quad plate package (QFPs) and thin quad flat packages (TQFPs) have each a greatly increased number of pins.

Lead frames having inner leads arranged at small pitches among lead frames for semiconductor packages are 20 fabricated by a photolithographic etching process, while lead frames having inner leads arranged at comparatively large pitches among lead frames for semiconductor packages are fabricated by press working. However, lead frames having a large number of fine inner leads to be used for 25 forming semiconductor packages having a large number of

pins are fabricated by subjecting a blank of a thickness on the order of 0.25 mm to an etching process, not a press working.

5 The etching process for forming a lead frame having fine inner leads will be described hereinafter with reference to FIG. 14. First, a copper alloy or 42 alloy thin sheet of a thickness on the order of 0.25 mm (a lead frame blank 1410) is cleaned perfectly (FIG. 14(a)). Then, 10 a photoresist, such as a water-soluble casein photoresist containing potassium dichromate as a sensitive agent, is spread in photoresist films 1420 over the major surfaces of the thin film as shown in FIG. 14(b).

15 Then, the photoresist films are exposed, through a mask of a predetermined pattern, to light emitted by a high-pressure mercury lamp, and the thin sheet is immersed in a developer for development to form a patterned photoresist film 1430 as shown in FIG. 14(c). Then, the thin sheet is subjected, when need be, to a hardening process, a washing process and such, and then an etchant 20 containing ferric chloride as a principal component is sprayed against the thin sheet 1410 to etch through portions of the thin sheet 1410 not coated with the patterned photoresist films 1420 so that inner leads of predetermined sizes and shapes are formed as shown in FIG. 25 14(d).

Then, the patterned resist films are removed, the patterned thin sheet 1410 is washed to complete a lead frame having the inner leads of desired shapes as shown in FIG. 14(e). Predetermined areas of the lead frame thus formed by the etching process are silver-plated. After being washed and dried, an adhesive polyimide tape is stuck to the inner leads for fixation, predetermined tab bars are bent, when need be, and the die pad depressed. In the etching process, the etchant etches the thin sheet in both the direction of the thickness and directions perpendicular to the thickness, which limits the miniaturization of inner lead pitches of lead frames. Since the thin sheet is etched from both the major surfaces as shown in FIG. 14 during the etching process, it is said, when the lead frame has a line-and-space shape, that the smallest possible intervals between the lines are in the range of 50 to 100 $\mu$  of the thickness of the thin sheet. From the viewpoint of forming the outer lead having a sufficient strength, generally, the thickness of the thin sheet must be about 0.125 mm or above. Furthermore, the width of the inner leads must be in the range of 70 to 80  $\mu$ m for successful wire bonding. When the etching process as illustrated in FIG. 14 is employed in fabricating a lead frame, a thin sheet of a small thickness in the range of 0.125 to 0.15 mm is used and inner leads are formed by etching so that the

fine tips thereof are arranged at a pitch of about 0.1 mm.

However, recent miniature resin-encapsulated semiconductor package requires inner leads arranged 5 pitches in the range of 0.13 to 0.15 mm, far smaller to 0.165 mm. When a lead frame is fabricated by processing thin sheet of a reduced thickness, the strength of outer leads of such a lead frame is not large enough 10 to withstand external forces that may be applied thereto in the subsequent processes including an assembling process and a chip mounting process. Accordingly, there is a limit to the reduction of the thickness of the thin sheet to enable the fabrication of a minute lead frame having fine 15 leads arranged at very small pitches by etching.

An etching method previously proposed to overcome such difficulties subjects a thin sheet to an etching process to form a lead frame after reducing the thickness of portions of the thin sheet corresponding to the inner leads of the lead frame by half-etching or pressing to form 20 the fine inner leads by etching without reducing the strength of the outer leads. However, problems arise in accuracy in the subsequent processes when the lead frame is formed by etching after reducing the thickness of the portions corresponding to the inner leads by pressing; for 25 example, the smoothness of the surface of the plated areas

is unsatisfactory, the inner leads cannot be formed in a flatness and a dimensional accuracy required to clamp the lead frame accurately for bonding and molding, and a platemaking process must be repeated twice making the lead fabricating process intricate. It is also necessary to repeat a platemaking process twice when the thickness of the portions of the thin sheet corresponding to the inner leads is reduced by half etching before subjecting the thin sheet to an etching process for forming the lead frame, which also makes the lead frame fabricating process intricate. Thus, this previously proposed etching method has not yet been applied to practical lead frame fabricating processes.

15 (SUBJECT MATTERS TO BE SOLVED BY THE INVENTION)

On the other hand, because a pitch among inner leads is made narrow as the number of terminals is increased, it is considered important to know whether a problem is caused or not in association with position shift or coplanarity of an outer lead when implementing a chip mounting process. Accordingly, the present invention has been made in an effort to solve the problems occurring in the related art, and an object of the present invention is to provide a resin-encapsulated semiconductor device capable of meeting the requirement for an increase in the number of terminals

and resolving problems which are caused in assoc:  
position shift and coplanarity of an outer lead.

(MEANS FOR SOLVING THE SUBJECT MATTERS)

5 According to one aspect of the present invention there is provided a resin-encapsulated semiconductor using a lead frame which is shaped in accordance with a two-step etching process to a body wherein a thickness of the inner leads is less than that of the lead frame comprising: inner leads having the thickness less than that of the lead frame blank; and terminal columns 10 connected to the inner leads and having the same thickness as that of the lead frame blank, the terminal columns being of a column-shaped configuration which is adapted 15 electrically connected to an external circuit, the columns being disposed outside of the inner lead frame manner such that they are coupled to the inner lead direction orthogonal to the thickness-wise direction thereof, the terminal columns having terminal portions 20 arranged on top ends thereof, the terminal portions being made of solders, etc. and exposed to the outside beyond the resin encapsulate, outer surfaces of the terminal columns also being exposed to the outside beyond the 25 encapsulate, each inner lead possessing a rectangular cross-section and having four surfaces including a

surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surface of a remaining portion of the inner lead having the same thickness with the lead frame blank while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

According to another aspect of the present invention there is provided a resin-encapsulated semiconductor device using a lead frame which is shaped in accordance with a two-step etching process to a body wherein a thickness of inner leads is less than that of the lead frame blank comprising: inner leads having the thickness less than that of the lead frame blank; and terminal columns integrally connected to the inner leads and having the same thickness with the lead frame blank, the terminal columns possessing a column-shaped configuration which is adapted to be electrically connected to an external circuit, the terminal columns being disposed outside of the inner leads in a manner such that they are coupled to the inner leads in a direction orthogonal to the thickness-wise direction thereof, portions of top ends of the terminal columns being exposed to the outside beyond a resin encapsulate, outer surfaces of the terminal columns also being exposed to the outside beyond the resin encapsulate, each inner lead

possessing a rectangular cross-section and having four surfaces including a first surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surface of a remaining portion of the 5 inner lead having the same thickness with the lead frame blank while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

According to another aspect of the present invention, 10 a semiconductor chip is received inward of the inner leads, and electrodes (pads) of the semiconductor chip are electrically connected to the inner leads through wires, respectively. According to another aspect of the present invention, the lead frame has a die pad, and the 15 semiconductor chip is mounted onto the die pad. According to another aspect of the present invention, the lead frame does not have a die pad, and the semiconductor chip is fastened to the inner leads using a reinforcing fastener tape. According to still another aspect of the present 20 invention, the semiconductor chip is fastened by means of insulating adhesive to the second surfaces of the inner leads on one surface thereof on which the electrodes are located, and the electrodes of the semiconductor chip are electrically connected to the first surfaces of the inner 25 leads through wires, respectively. According to yet still

another aspect of the present invention, the semiconductor chip is fastened to the second surfaces of the inner leads by bumps thereby to be electrically connected to the inner leads. In the above descriptions, in the case that the terminal columns have terminal portions which are arranged on top ends of the terminal columns, with the terminal portions made of solders, etc. and exposed to the outside beyond the resin encapsulate, while it is the norm that the terminal portions comprising the solders, etc. are exposed to the outside beyond the resin encapsulate, it is not necessarily required for the terminal portions to be projected beyond the resin encapsulate. Moreover, while it is possible to use the outside surfaces of the terminal columns while they are not encapsulated by the resin encapsulate and they are exposed to the outside, the outside surfaces of the terminal columns which are not encapsulated by the resin encapsulate, can be covered by a protective frame using adhesive, etc.

20 (WORKING FUNCTIONS)

The resin-encapsulated semiconductor device in accordance with the present invention can meet a demand for an increase in the number of terminals. At the same time, in the resin-encapsulated semiconductor device, because the forming process of the outer leads as in the case of using

2 mono-layered lead frame shown in FIG. 13(B) is not required, it is possible to provide a semiconductor device in which no problems are caused in association with position shift and coplanarity of the outer leads. More particularly, the use of a multi-pinned lead frame shaped in a manner that inner leads have a thickness less than that of the lead frame blank by a two-step etching process, that is, the inner leads are arranged at a fine pitch, can meet a demand for an increase in the pin number of the 10 semiconductor device. Furthermore, by using the lead frame which is fabricated by a two-step etching process as will be described later with reference to FIG. 1, the second surface of each inner lead has coplanarity, and is excellent in wire-bonding property. In addition, since the 15 first surface of the inner lead is also a flat surface and the third and fourth surfaces are depressed toward the inside of the inner lead, the inner leads are stable and coplanarity width upon wire bonding -process can be enlarged.

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#### (EMBODIMENTS)

Embodiments of the resin-encapsulated semiconductor device in accordance with the present invention will now be described with reference to the attached drawings. First, 25 a resin-encapsulated semiconductor device in accordance

with a first embodiment of the present invention described hereinafter with reference to FIGS. 1-3. FIG. 1(a) is a cross-sectional view of the encapsulated semiconductor device according to the embodiment of the present invention. FIG. 1(b) is a sectional view of an inner lead taken along the line of FIG. 1(a), and FIG. 1(c) is a cross-sectional view of a terminal column taken along the line 51-52 of FIG. 1(a). Moreover, FIG. 2(a) is a perspective view of the encapsulated semiconductor device according to the embodiment of the present invention, FIG. 2(b) is a view of the resin-encapsulated semiconductor device of FIG. 2(a), and FIG. 2(c) is a bottom view of the encapsulated semiconductor device of FIG. 2(a). In FIGS. 1 and 2, a drawing reference numeral 100 represents an encapsulated semiconductor device, 110 a semiconductor chip, 111 electrodes (pads), 120 wires, 130 a lead, 131 inner leads, 131Aa a first surface, 131Ab a second surface, 131Ac a third surface, 131Ad a fourth surface, 133 terminal columns, 133A terminal portions, 133B surfaces, 133S a top surface, 135 a die pad, and 140 a resin encapsulate.

In the resin-encapsulated semiconductor device according to the first embodiment, as shown in FIG. 2(a), the semiconductor chip 110 is placed inward of the lead 130.

leads 131. As can be readily seen from FIG. 1(a), the semiconductor chip 110 is mounted on the die pad 133 at one surface thereof which is opposed to the other surface thereof where the electrodes pads 101 of the semiconductor chip 110 are arranged. Each electrode pad 101 is electrically connected to the second surface 131B of the inner lead 131 through the wire 120. The electrical connection between the resin-encapsulated semiconductor device 100 of this embodiment and an external circuit is achieved by mounting the resin-encapsulated semiconductor device 100 via the terminal portions 133A each being made of a semi-spherical solder, on a printed circuit substrate, with the terminal portions 133A located on the top surfaces 133S of the terminal columns 133, respectively. In the resin-encapsulated semiconductor device of the first embodiment of the present invention, it is not necessarily required to provide a protective frame 190, and instead, a structure, as shown in FIG. 1(d), in which no protective frame is used can be adopted.

The lead frame 130 used in the semiconductor device 100 according to the first embodiment is made of a 42% nickel-zinc alloy. Therefore, the lead frame 130A which has a contour as shown in FIG. 9(a) and is shaped by an etching process, is used as the lead frame 130. The lead frame 130 has inner leads 131 which are shaped to have a

thickness less than that of the terminal columns 133 at other portions. Dam bars 136 serve as a dam when encapsulating the semiconductor chip 110 with a resin. Moreover, although the lead frame 130A which is processed by etching to have the contour as shown in FIG. 1(a) is used in this embodiment, the lead frame is not limited to such a contour because portions except the inner leads 131 and the terminal columns 133 are not necessary. The inner leads 131 have a thickness of 40 mm whereas the portions 10 of the lead frame 130 other than the inner leads 131 have a thickness of 0.15 mm which corresponds to the thickness of the lead frame blank. The other portions of the lead frame 130 except the inner leads 131 may not have the thickness of 0.15 mm, but have a thickness of 0.125 mm-0.50 mm which 15 is thinner. The tips of the inner leads 131 have a small pitch of 0.12 mm so as to achieve an increase in the number of terminals for semiconductor devices. The second face 131Ab of the inner lead 131 has a substantially flat profile so as to allow an easy wire bonding thereon. Also, 20 as shown in FIG. 1(b), because the third and fourth faces 131Ac and 131Ad have a concave shape which is depressed toward the inside of the associated inner lead, a high strength can be obtained even though the second face (wire bonding surface) 131Ab is narrowed.

25 In the present embodiment, since twisting does not

occur in the inner leads 131 irrespective of whether the inner leads 131 is long or not. The inner leads having the contour, as shown in FIG. 9(a), in which the tips of the inner leads 131 are separated one from another, are prepared by the etching process, and the inner leads are resin-encapsulated after mounting the semiconductor chip thereon as will be described later. However, where the inner leads 131 are long in their length and have a tendency for the generation of twisting therein, it is impossible to fabricate the lead frame by etching to have the contour as shown in FIG. 9(a). Therefore, after etching the lead frame in a state where the tips of the inner leads are fixed to the connecting portion 131B as shown in FIG. 9(c)(1), the inner leads 131 are fixed with the reinforcing tape 160 as shown in FIG. 9(c)(D). Then, the connecting portions 131B which are not necessary in the fabrication of the resin-encapsulated semiconductor device are removed by a press as shown in FIG. 9(c)(11), and a semiconductor device is then mounted on the lead frame.

Hereinafter, a method for the fabrication of the resin-encapsulated semiconductor device will now be described with reference to FIG. 8. First, the lead frame 130A, as shown in FIG. 9(a), which is shaped by the etching process as will be described later, is prepared such that the second surfaces 131Ab of the inner leads 131 are

directed upward (FIG. 8(a)).

Then, the semiconductor chip 110 is mounted onto the die pad 135 such that the surfaces of the semiconductor chip 110 on which the electrodes 111 are arranged, are 5 directed upward (FIG. 8(b)).

Next, after the semiconductor chip 110 is fastened onto the die pad 135, the electrodes 111 of the semiconductor chip 110 and the second surfaces 131A**b** of the inner leads 131 are bonded with each other using wires 120 10 (FIG. 8(c)).

Subsequently, encapsulation is carried out with the conventional resin encapsulate 140. Thereafter, unnecessary portions of the lead frame 130 which are protruded from the resin encapsulate 140 are cut by a press 15 to form terminal columns 133 and also the side surfaces 133B of the terminal columns 133 (FIG. 8(d)).

Then, the dam bars 136, the frame portions 137, etc. of the lead frame 130A as shown in FIG. 9 are removed. Next, the terminal portions 133A each made of the semi- 20 spherical solder are arranged on the outer surface of each terminal column 133 to fabricate a resin-encapsulated semiconductor device (FIG. 8(e)).

Thereafter, the protective frame 180 is arranged by means of adhesive around an entire outer surface of the 25 resultant structure in such a manner that the side surfaces

of the terminal columns 133 are covered thereby (FIG. 6(f)). At this time, the protective frame 180 functions to reinforce the semiconductor device. In other words, the protective frame 180 serves to prevent moisture from leaking into a gap between the resin encapsulate and the terminal columns due to the fact that the side surfaces of the terminal columns are exposed to the outside, whereby a crack is not formed in the semiconductor device and the breakage of the semiconductor device is avoided. However, persons skilled in the art will readily appreciate that it is not necessarily required to provide the protective frame 180. Also, when such an encapsulating process by the resin is carried out using a desired mold, the encapsulating process is implemented in a state wherein the outer side surfaces of the terminal columns of the lead frame are somewhat protruded out of the resin encapsulate.

A method for etching the lead frame of the first embodiment will now be described in conjunction with the attached drawings. FIG. 11 is of cross-sectional views respectively illustrating sequential steps of the etching process for the lead frame of the first embodiment. In particular, the cross-sectional views of FIG. 1 correspond to a cross section taken along the line D1-D2 of FIG. 9(a). In FIG. 11, the reference numeral 1110 denotes a lead frame blank, 1120A and 1120B resist patterns, 1130 first opening,

1140 second openings, 1150 first concave portions, 1160 second concave portions, 1170 flat surfaces, and 1180 an etch-resistant layer. First, a water-soluble casein resist using potassium dichromate as a sensitive agent is coated over both surfaces of the lead frame blank 1110 made of a 42% nickel-iron alloy and having a thickness of about 0.13 mm. Using desired pattern plates, the resist films are patterned to form resist patterns 1120A and 1120B having first opening 1130 and second openings 1140, respectively 5 (FIG. 11(a)).

The first opening 1130 is adapted to etch the lead frame blank 1110 to have a flat etched bottom surface to a thickness smaller than that of the lead frame blank 1110 in a subsequent process. The second openings 1140 are adapted 15 to form desired shapes of tips of inner leads. Although the first opening 1130 includes at least an area forming the tips of the inner leads 1110, a topology generated by partially thinned portion by etching in a subsequent process can cause hindrance in a taping process or a clamping process for fixing the lead frame. Thus, an area 20 to be etched needs to be large without being limited to fine portions of the tips of the inner leads. Thereafter, both surfaces of the lead frame blank 1110 formed with the resist patterns are etched using a 48 Be' ferric chloride 25 solution of a temperature of 57°C at a spray pressure of

2.5 kg/cm<sup>2</sup>. The etching process is terminated at the point of time when first recesses 1150 etched to have a flat etched bottom surface have a depth  $h$  corresponding to  $1/3$  of the thickness of the lead frame blank (FIG. II (c)).

5        Although both surfaces of the lead frame blank 1110 are simultaneously etched in the primary etching process, it is not necessary to simultaneously etch both surfaces of the lead frame blank 1110. The reason why both surfaces of the lead frame blank 1110 are simultaneously etched, as in 10      this embodiment, is to reduce the etching time taken in a secondary etching process as will be described later. The total time taken for the primary and secondary etching processes is less than that taken in the case of etching of only one surface of the lead frame blank on which the 15      resist pattern 1120B is formed. Subsequently, the surface provided with the first recesses 1150 respectively etched at the first opening 1130 is entirely coated with an etch-resistant hot-melt wax (acidic wax type MR-WB6, The Incotec Inc.) by a die coater to form an etch-resistant 20      layer 1180 so as to fill up the first recesses 1150 and to cover the resist pattern 1120A (FIG. II(c)).

25      It is not necessary to coat the etch-resistant layer 1180 over the entire portion of the surface provided with the resist pattern 1120A. However, it is preferred that the etch-resistant layer 1180 be coated over the entire

portion of the surface formed with the first recess 5 and first opening 1130, as shown in FIG. 11(c), because it is difficult to coat the etch-resistant layer 1180 on the surface portion including the first recesses. Although the etch-resistant layer 1180 was employed in this embodiment as an alkali-soluble wax, any surface-resistant to the etching action of the etchant solution remaining somewhat soft during etching may be used. For forming the etch-resistant layer 1180 is not limited to the above-mentioned wax, but may be a wax of a UV-type. Since each first recess 1150 etched by the primary etching process at the surface formed with the part adapted to form a desired shape of the inner lead is filled up with the etch-resistant layer 1180, it is further etched in the following secondary etching process. The etch-resistant layer 1180 also enhances the mechanical strength of the lead frame blank for the second etching process, thereby enabling the second etching process to be conducted while keeping a high accuracy. It is possible to enable a second etchant solution to be sprayed at an increased spraying pressure, for example, 2.5 kg or above, in the secondary etching process. The increased spraying pressure promotes the progress of etching in direction of the thickness of the lead frame blank in the secondary etching process. Then, the lead frame blank

portion of the surface formed with the first recess 1130 and first opening 1130, as shown in FIG. 11(c), because it is difficult to coat the etch-resistant layer 1160 on the surface portion including the first recesses 1130. Although the etch-resistant layer 1160 was employed in this embodiment as an alkali-soluble wax, any substance resistant to the etching action of the etchant solution remaining somewhat soft during etching may be used. For forming the etch-resistant layer 1160 is not limited to the above-mentioned wax, but may be a wax of a UV-type. Since each first recess 1130 etched by the primary etching process at the surface formed with the part adapted to form a desired shape of the inner lead is filled up with the etch-resistant layer 1160, it is further etched in the following secondary etching process. The etch-resistant layer 1160 also enhances the mechanical strength of the lead frame blank for the second etching process, thereby enabling the second etching process to be conducted while keeping a high accuracy. It is possible to enable a second etchant solution to be sprayed at an increased spraying pressure, for example, 2.5 kg or above, in the secondary etching process. The increased spraying pressure promotes the progress of etching in direction of the thickness of the lead frame blank in the secondary etching process. Then, the lead frame blank

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surfaces 131Aa of the tips of the inner leads as shown in FIG. 1, are flushed with one surfaces of remaining portions of the inner leads having the same thickness with the lead frame while being opposed to the second surfaces 131Ab, and the third and fourth surfaces are formed to have a concave shape which is depressed toward the inside of the inner leads. Where a semiconductor chip is mounted on the second surfaces 131Ab of the inner leads by means of bumps for an electrical connection therebetween, as in a semiconductor device according to a third embodiment as will be described hereinafter, an increased tolerance for the connection by bumps is obtained when the second surface 131Ab has a concave shape depressed toward the inside of the inner lead. To this end, an etching method shown in FIG. 12 is adopted in this case. The etching method shown in FIG. 12 is the same as that of FIG. 11 in association with its primary etching process. After completion of the primary etching process, the etching method is conducted in a manner different from that of the etching method of FIG. 11 in that the second etching process is conducted at the side of the first recesses 1150 after filling up the second recesses 1160 by the etch-resist layer 1180, thereby completely perforating the second recesses 1160. At this time, by implementing the primary etching process, etching at the side of the second openings 1140 is performed in a

sufficient manner. The cross section of each inner lead, including its tip, formed in accordance with the etching method of FIG. 12, has a concave shape depressed toward the inside of the inner lead at the second surface 131a<sub>2</sub>, as shown in FIG. 6(b).

The etching method in which the etching process is conducted at two separate steps, respectively, as in that of FIGS. 11 and 12, is generally called a "two-step etching method". This etching method is advantageous in that a desired fineness can be obtained. The etching method used to fabricate the lead frame 130A of the first embodiment shown in FIG. 9 involves the two-step etching method and the method for forming a desired shape of each lead frame portion while reducing the thickness of each pattern formed. In particular, the etching method makes it possible to achieve a desired fineness. In accordance with the method illustrated in FIGS. 11 and 12, the fineness of the tip of each inner lead 131A formed by this method is dependent on the shape of the second recesses 1160 and the thickness  $t$  of the inner lead tip which is finally obtained. For example, where the blank has a thickness  $t$  reduced to 50  $\mu\text{m}$ , the inner leads can have a fineness corresponding to a lead width  $W_1$  of 100  $\mu\text{m}$  and a tip pitch  $p$  of 0.15 mm, as shown in FIG. 11(e). In the case of using a small blank thickness  $t$  of about 30  $\mu\text{m}$  and a lead

width  $W_1$  of 70  $\mu\text{m}$ , it is possible to form inner leads having a fineness corresponding to an inner lead pitch  $p$  of 0.12  $\mu\text{m}$ . Of course, it may be possible to form inner leads having a further reduced tip pitch by adjusting the blank thickness  $t$  and the lead width  $W_1$ . That is to say, an inner lead tip pitch  $p$  up to 0.08  $\mu\text{m}$ , a blank thickness  $t$  up to 25  $\mu\text{m}$ , and a lead width  $W_1$  up to 40  $\mu\text{m}$  can be obtained.

In the case where twisting of the inner leads does not occur in the fabricating process, as in the case where the inner leads are short in their length, a lead frame illustrated in FIG. 9(a) can be directly obtained. However, where the inner leads are long in length as compared to those of the first embodiment, the inner leads have tendency for the generation of twisting. Thus, in this case, the lead frame is obtained by etching in a state where the tips of the inner leads are bound to each other by a connecting member 131B as shown in FIG. 9(c)(1). Then, the connecting member 131B which is not necessary for the fabrication of a semiconductor package is cut off by means of a press to obtain a lead frame shaped as shown in FIG. 9(a).

Moreover, as described above, where unnecessary portions in a structure shown in FIG. 9(c)(1) are cut to obtain the lead frame having the contour shown in FIG.

9(a), a reinforcing tape 160 (a polyimide tape is generally used, as shown in FIG. 9(c)(a)). While the connecting member 131B is cut off by means of a press to obtain the contour shown in FIG. 9(c)(b), a semiconductor device is mounted on the lead frame still having the reinforcing tape attached thereto. Also, the mounted semiconductor device is encapsulated with a resin in a condition where the lead frame still has the tape. The line E11-E12 illustrates a cut portion.

10 The tip of the inner lead 131 of the lead frame used in the semiconductor device of this first embodiment has a cross-sectional shape as shown in FIG. 13(1)(a). The tip 131A has an etched flat surface (second surface) 131AB which is substantially flat and therefore has a width  $W_1$  slightly greater than the width  $W_2$  of an opposite surface. The widths  $W_1$  and  $W_2$  (about 1000  $\mu$ m) are more than the width  $W$  at the central portion of the tips when viewed in the direction of the inner lead thickness. Thus, the tip of the inner lead has a cross-sectional shape having opposite wide surfaces. To this end, although either of the opposite surfaces of the tip 131A can be easily electrically connected to a semiconductor device (not shown) by a wire 120A or 120B, this embodiment illustrates the use of the etched flat surface for wire-bonding as shown in FIG. 13(1)(a). In FIG. 13, a reference numeral

131Ab depicts an etched flat surface, 131Aa a surface of a lead frame blank, and 121A and 121B, respectively, a plated portion. In the case of FIG. 13(B)(a), there has particularly excellent in wire-bonding property, because the etched flat surface does not have roughness. FIG. 13(B) shows that the tip 1331B of the inner lead of the lead frame fabricated according to the process illustrated in FIG. 14 is wire-bonded to a semiconductor device. In this case, however, both the opposite surfaces of the tip 10 1331B of the inner lead are flat, but have a width smaller than that in a direction of the inner lead thickness. In addition to this, as both the opposite surfaces of the tip 1331B is formed of surfaces of the lead frame blank, these surfaces have an inferior wire-bonding property as compared 15 to that of the etched flat surface of this first embodiment. FIG. 13(B) shows that the inner lead tip 1331C or 1331D, obtained by thinning in its thickness by a means of a press (coining) and then by etching, is wire-bonded to a semiconductor device (not shown). In this 20 case, however, a pressed surface of the inner lead tip is not flat as shown FIG. 13(B). Thus, the wire-bonding on either of the opposite surfaces as shown in FIG. 13(B)(a) or FIG. 13(B)(b) often results in an insufficient wire-bonding stability and a problematic quality. The drawing 25 reference numeral 1331Ab represents a coining surface.

A modified example of the resin-encapsulated semiconductor device in accordance with the first embodiment of the present invention will be described hereinafter. FIGS. 3(a) through 3(e) are cross-sectional views of the modified example of the resin-encapsulated semiconductor device in accordance with the first embodiment of the present invention. The semiconductor device of the modified example as shown in FIG. 3(a), is different from that of the first embodiment in that a position of the die pad 135 is changed, that is, the die pad 135 is exposed to the outside. By the fact that the die pad 135 is exposed to the outside, the heat dissipation property is improved as compared to the first embodiment. Also, in the semiconductor device of the modified example as shown in FIG. 3(b), because the die pad 135 is exposed to the outside, the heat dissipation property is improved as compared to the first embodiment. Unlike the first embodiment or the modified example as shown in FIG. 3(a), in the present modified example as shown in FIG. 3(b), because a direction of the semiconductor device 110 is changed, the first surfaces of the lead frame are established as the wire bonding surfaces. The modified examples as shown in FIGS. 3(c), 3(d) and 3(e), illustrate semiconductor devices which are obtained by modifying the semiconductor devices of the first embodiment, the modified

example as shown in FIG. 3(a) and the modified example as shown in FIG. 3(b), wherein the semi-spherical solders are not used, and instead, the top surfaces of the terminal columns are directly used as the terminal portions, whereby an entire manufacturing procedure can be simplified.

Next, a resin-encapsulated semiconductor device in accordance with a second embodiment of the present invention will be described. FIG. 4(a) is a cross-sectional view of the resin-encapsulated semiconductor device in accordance with the second embodiment of the present invention, FIG. 4(b) is a cross-sectional view illustrating inner leads, taken along the line A3-A4 of FIG. 4(a), and FIG. 4(c) is a cross-sectional view illustrating a terminal column, taken along the line B3-B4 of FIG. 4(a). Because an outer appearance of the semiconductor device of the second embodiment is substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 3, the drawing reference numeral 200 represents a semiconductor device, 210 a semiconductor chip, 211 electrodes (pads), 220 wires, 230 a lead frame, 231 inner leads, 231Ab a second surface, 231Ac a third surface, 231Ad a fourth surface, 233 terminal columns, 233A terminal portions, 233B side surfaces, 233S top surfaces, 240 a resin encapsulate, and 270 a reinforcing fastener tape. In the semiconductor device of

this second embodiment, the lead frame 230 does not have a die pad, the semiconductor chip 210 is fastened to the inner leads 231 by the reinforcing fastener tape 270, and the semiconductor chip 210 is electrically connected at its electrodes (pads) 211 to the second surfaces 231Ab of the inner leads 231 by wires 220. Also, in the case of this second embodiment, similarly to the first embodiment, the electrical connection between the resin-encapsulated semiconductor device 200 of this embodiment and an external circuit is achieved by mounting the resin-encapsulated semiconductor device 200 via the terminal portions 233A each being made of a semi-spherical solder, on a printed circuit substrate, with the terminal portions 233A located on the top surfaces 233S of the terminal columns 233, respectively.

In addition, the semiconductor device of this second embodiment does not have a die pad as shown in FIGs. 10(a) and 10(b). The manufacturing method of the semiconductor device of this embodiment using the lead frame 230A which is shaped by the etching process is substantially the same as that of the first embodiment except that, while in the case of the first embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip is fastened to the inner leads, in the case of the second embodiment, the wire

bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip 210 is fastened together with the inner leads 230 by the reinforcing fastener tape 260. Also, the cutting process 5 for the unnecessary portions and the terminal portion forming process after resin encapsulating process are implemented in the same way as the first embodiment. The lead frame 230 as shown in FIG. 10(a) is obtained in the same manner by which the lead frame 130A as shown in FIG. 9(a) is obtained. In other words, by cutting the resultant structure obtained after etching the structure as shown in FIG. 10(c)(1), the contour as shown in FIG. 10(a) is obtained. At this time, the conventional reinforcing fastener tape 260 (the polyimide tape) as shown in FIG. 10(c)(□), which performs a reinforcing function is used. 10 15 20 25

FIG. 5(a) through 5(c) are cross-sectional views illustrating modified examples of the semiconductor device of the second embodiment. The semiconductor device as shown in FIG. 5(a) is different from the semiconductor device of the second embodiment, in that the surface of the semiconductor chip thereof which has the electrodes is directed downward. The modified examples as shown in FIGs. 5(b) and 5(c), illustrate semiconductor devices which are obtained by modifying the semiconductor devices of the second embodiment and the modified example as shown in FIG.

5(a), wherein the semi-spherical solders are not used, and instead, the top surfaces of the terminal columns are directly used as the terminal portions. In these examples, because a protective frame is not used and the side 5 surfaces 333B of the terminal columns 333 are exposed to the outside, a checking operation by a test, etc. can be easily performed.

Hereinafter, a resin-encapsulated semiconductor device in accordance with a third embodiment of the present invention will be described. FIG. 6(a) is a cross-sectional view of the resin-encapsulated semiconductor device of the third embodiment, FIG. 6(b) is a cross-sectional view illustrating inner leads, taken along the line A5-A6 of FIG. 6(a), and FIG. 6(c) is a cross-sectional view illustrating a terminal column, taken along the line B5-B6 of FIG. 6(b). Because an outer appearance of the semiconductor device of this third embodiment is substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 6, the drawing reference numeral 300 represents a semiconductor device, 310 a semiconductor chip, 312 bumps, 330 a lead frame, 331 inner leads, 331Aa a first surface, 331Ab a second surface, 331Ac a third surface, 331Ad a fourth surface, 333 terminal columns, 333A terminal portions, 333B side surfaces, 333S top surfaces, 340 a resin encapsulate, and 350 a

reinforcing fastener tape. In the semiconductor device of this third embodiment, the semiconductor chip 310 is fastened to the second surfaces 331Ab of the inner leads 331 by the bumps 311 thereby to be electrically connected to the second surfaces 331Ab. The lead frame 330 has a contour as shown in FIGs. 10(a) and 10(b), which is formed by the etching process of FIG. 11. As shown in FIG. 13(1)(b), both widths W1A and W2A (about 100  $\mu$ m) at top and bottom ends of the inner leads 331 are larger than a width W3A at a center portion in a thickness-wise direction. Due to the fact that the second surfaces 331Ab of the inner leads 331 is depressed toward the inside of the inner leads and the first surfaces 331Aa are flat, a desired fineness can be obtained. Also, when the second surfaces 331Ab of the inner leads 331 are electrically connected to the semiconductor chip via bumps, easy connection can be accomplished as shown in FIG. 13(2)(b). Further, in the case of this third embodiment, as in the case of the first and second embodiments, the electrical connection between the resin-encapsulated semiconductor device 300 of this embodiment and an external circuit is achieved by mounting the resin-encapsulated semiconductor device 300 via the terminal portions 333A each being made of a semi-spherical solder, on a printed circuit substrate, with the terminal portions 333A located on the top surfaces of the terminal

columns 333, respectively.

In addition, unlike the semiconductor device of the first embodiment, the semiconductor device of this third embodiment uses a lead frame which is shaped by the etching process as shown in FIG. 12. However, the manufacturing method of the semiconductor device of this embodiment is substantially the same as that of the first embodiment except that, while in the case of the first embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip is fastened to the inner leads, in the case of this third embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip 310 is fastened to the inner leads 331 via the bumps. Also, the cutting process for the unnecessary portions and the terminal portion forming process after resin encapsulating process are implemented in the same way as the first embodiment.

FIG. 6(d) is a cross-sectional view illustrating a modified example of the semiconductor device in accordance with the third embodiment of the present invention. In the modified example of the semiconductor device as shown in FIG. 6(d), the terminal portions each comprising the semi-spherical solder are not provided, and the top surfaces of the terminal columns are directly used as the terminal

positions. Because the protective frame is not used and the side surfaces 333B of the terminal columns 333 are exposed to the outside, a checking operation by a test, etc. can be easily performed.

5       Hereinafter, a resin-encapsulated semiconductor device in accordance with a fourth embodiment of the present invention will be described. FIG. 7(a) is a cross-sectional view of the resin-encapsulated semiconductor device of the fourth embodiment, FIG. 7(b) is a cross-sectional view illustrating inner leads, taken along the line A7-A8 of FIG. 7(a), and FIG. 7(c) is a cross-sectional view illustrating a terminal column, taken along the line B7-B8 of FIG. 7(b). Because an outer appearance of the semiconductor device of this fourth embodiment is substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 7, the drawing reference numeral 400 represents a semiconductor device, 410 a semiconductor chip, 411 pads, 430 a-lead frame, 431 inner leads, 431Aa a first surface, 431Ab a second surface, 431Ac a third surface, 431Ad a fourth surface, 433 terminal columns, 433A terminal portions, 433B side surfaces, 433S top surfaces, 440 a resin encapsulate, and 470 insulating adhesive. In the semiconductor device of this fourth embodiment, one surface of the semiconductor chip 410 on which the pads 411 are disposed is fastened to the second

surfaces 431AB of the inner leads 431 by the insul. adhesive 470, and the pads 411 and the first surfaces of the inner leads 431 are electrically connected with other by wires 420. The semiconductor device of 5 fourth embodiment uses the same lead frame which is use the third embodiment, which has the contour as shown FIG. 10(a) and 10(b). Also, in the case of this embodiment, as in the case of the first and sec 10 embodiments, the electrical connection between the res encapsulated semiconductor device 400 of this embodiment and an external circuit is achieved by mounting the res encapsulated semiconductor device 400 via the terminal portions 433A each being made of a semi-spherical solder on a printed circuit substrate, with the terminal portion 15 433A located on the top surfaces of the terminal column 433, respectively.

FIG. 7(d) is a cross-sectional view illustrating modified example of the semiconductor device in accordance with the fourth embodiment of the present invention. 20 the modified example of the semiconductor device as shown in FIG. 7(d), the terminal portions each comprising the semi-spherical solder are not provided, and the top surfaces of the terminal columns are directly used as the terminal portions. Because the protective frame is not 25 used and the side surfaces 433B of the terminal columns 433

are exposed to the outside, a checking operation by a test, etc. can be easily performed.

(EFFECTS OF THE INVENTION)

5 The present invention provides a resin-encapsulated semiconductor device employing the above-mentioned lead frame, which is capable of meeting a demand for the increased terminal number. Furthermore, the resin-encapsulated semiconductor device in accordance with this invention does not require a process of cutting or bending the dam bars as in the case of using a lead frame having outer leads as shown in FIG. 13(b). As a result of this, 10 the resin-encapsulated semiconductor device does not have a problem in that the outer leads are bent, or a problem associated with coplanarity. In addition to these 15 advantages, the resin-encapsulated semiconductor device has a shortened interconnection length as compared to the QTP or the BGA, whereby the semiconductor device can be reduced in a parasitic capacity, and shortened in a transfer delay 20 time.

55:543 v:

55:543 v:



## (特許請求の範囲)

(請求項1) 2段ニッティング加工によりインナーリードの底面がリードフレームニッティング面よりも底面に加工されたリードフレームを用いた電子部品であつて、前記リードフレームは、リードフレーム素材よりも底面のインナーリードと、インナーリードに一骨筋に跨るしたリードフレームニッティング面と底面との外筋部と底面との底面の部材とを有し、且つ、該部材はインナーリードの外筋部においてインナーリードに対して底面万面に底面して抜けられており、該部材の元底面にキズ等からなる該部材を底面、該部材を外筋部と底面から底面をせ、該部材の外筋部の部材を外筋部と底面から底面をせおり、インナーリードは、底面部材が底面にて第1面、第2面、第3面、第4面の4面を有しており、かつ第1面はリードフレーム素材と同じ底面の部分の一方の面と底面にあつて第2面に向きており、第3面、第4面はインナーリードの内側に向かって凹んだ底面に底面をせていることを特徴とする底面封止型電子部品。

(請求項2) 2段ニッティング加工によりインナーリードの底面がリードフレームニッティング面よりも底面に加工されたリードフレームを用いた電子部品であつて、前記リードフレームは、リードフレーム素材よりも底面のインナーリードと、該インナーリードに一骨筋に跨るしたリードフレームニッティング面と底面との外筋部と底面との底面の部材とを有し、且つ、該部材はインナーリードの外筋部においてインナーリードに対して底面万面に底面して抜けられており、該部材の元底面の一骨筋を外筋部と底面から底面をせて該部材とし、該部材の外筋部の部材を外筋部と底面から底面をせしており、インナーリードは、底面部材が底面にて第1面、第2面、第3面、第4面の4面を有しており、かつ第1面はリードフレーム素材と同じ底面の部分の一方の面と底面にあつて第2面に向きており、第3面、第4面はインナーリードの内側に向かって凹んだ底面に底面をせていることを特徴とする底面封止型電子部品。

(請求項3) 特許権1ないし2において、半導体部子はインナーリード間に底面を有し、該半導体部子の底面部にワイヤにてインナーリードと底面に底面をせていることを特徴とする底面封止型電子部品。

(請求項4) ワイヤ1つにおいて、リードフレームにダイバッドを有しており、半導体部子にダイバッド上に底面を有し、底面をせていることを特徴とする底面封止型電子部品。

(請求項5) 特許権3において、リードフレームにダイバッドを有しないもので、半導体部子にインナーリードとともに底面封止用テープにより底面をせていることを特徴とする底面封止型電子部品。

(請求項6) 特許権1ないし2において、半導体部子は半導体部子の底面部の面をインナーリードの第2面

に施設なワイヤにより底面をせられており、且つ半導体部子の底面にワイヤによりインナーリードの第1面と底面に底面をせていることを特徴とする底面封止型電子部品。

(請求項7) 特許1ないし2において、半導体部子はパンプによりインナーリードの第2面に底面をせて底面にインナーリードとはしていをことを特徴とする底面封止型電子部品。

## (実用的新颖性)

## (0001)

(実用的新颖性) 本発明は、半導体部子の多面ニッティング面に外筋部と、且つ、アフターリードの底面ガレ(スニード)やアフターリードの底面(コブラナリティ)の凹凸による底面封止型電子部品。

## (0002)

(実用的新颖性) 特開15110号実用新案登録出願に、半導体部子(プラスチックリードフレームパッケージ)

は、一骨筋底面15110に示すかうな底面である。

ニスルテ15110を有するダイバッド15110の底面の底面との底面封止用を行つたアフターリード

15113、アフターリード15113に一骨筋に跨るした

インナーリード15112、該インナーリード15112の底面とニスルテ1520の底面パッド1521

とを多面的に底面するためのワイヤ1530、ニスルテ

1520を底面して底面からの底面、底面から底面

底面1520を底面しており、ニスルテ1520をリードフレームのダイバッド15111底面に底面したほ

に、底面1520により底面してパッケージとしたもの

で、ニスルテ1520の底面パッド1521に外筋で

底面のインナーリード15112を底面とすらものである。

そして、このような底面封止型の半導体部子の底面

封止して底面するためのワイヤ1530は、リードフレームは、一骨筋に底面15110に示すかうな底面のもので、ニスルテ

1511の底面に底面されたニスルテ部子と底面するためのインナーリード15112、該インナーリード15112に底面して外筋封止用底面を行つたアフターリード

15113、底面封止用のダムとなるダムバー15114

14、リードフレーム15110全体を底面するフレーム

(b)底面15115を底面して、逆元、カバール、 $\times$ 2倍率(42×ニッケル-60金)、丸元底面のような

底面に底面された底面を用い、プレス底面ししくはエッティング底面により底面していった。即、図15(b) (c)

に、図15(b) (d)に示すリードフレーム底面のF1-F2に底面する底面である。

(0003) このようなリードフレームを底面した底面

封止型の半導体部子(プラスチックリードフレームパッ

ケージ)において、ニスルテの底面底面の底面ヒニ

ニスルテの底面底面に底面、ト型封止型かつニスルテの

リード箔表面のエッチングによるルニッジが、これが原因とされていました。

18

(0005) これにお応じる方法として、アカマーリードの発達を促進したまま被削面を行なう方法で、インテリード部分をハーフニッティングもしくはプレスにより粗くしてニッティング加工を行なう方法が採用されていき..しかし、プレスにより粗くしてエッティングルニモるこなう場合には、仕工場においての風呂が不足する(例えは、カットニリアのモロロ)。ボンテンシテモールニジンケンのクランプに必要なインテリードのニモ性アモ風呂が不足されない。風呂を2段行なわなければならぬに至る。また浴槽エモが大きになら、水が漏れが多めある。そして、インテリード部分をハーフニッティングにより粗くしてエッティング加工を行なう方法の場合にも、ニモを2段行なわなければならず、製造工費が高めにならといふ点があり、いざれし实用化には、まだ至っていないのが現状であろう。

14. ~~4~~ ~~5~~ ~~6~~ ~~7~~ ~~8~~ ~~9~~ - 2 ? c 5

(58) エア栓の本体に止栓を固定するに、上元の止栓に取付することにより、リードフレームを取いたを取付するに於いて、多面子化に於いて、且つ、反対の図1 (b) に示す如きリードフレームを用いた場合の如きに、アフターリードのオーミングニードを設けしないもの、これらの中には既にアフターリードのスリューのない如きアフターリードのモード (コアラテリテナー) の状態を全くなくすことなく、また止栓の状態を可とすものである。又しくは、2枚エッチング板によりインテリードの底面が各面の端よりも又方に外側加工された、即ち、インテリードを2面に加工された多ビンのリードフレームを用いることにより、キヤノンの多面子化に於いても止栓の如きにより多面子化されたリードフレームを用いることにより、インテリードの又2面にテモドモテモ、ワイヤボンディング部の良いものとしている。又オーミング部で、又3面、又3面にインテリード部に止栓であるこのインテリード部に、止栓しておき、且つ、ワイヤボンディングのエンド部を止くこれら、0006:





まで深くすると、図11(c)に示す、厚さW1を1.0mmとして、インナーリード先端部ピッチ $\theta$ が0.15mmまで加工可能となる。厚さW1を1.0mm以上まで深くし、厚さW1を1.0mm以上とすると、インナーリード先端部ピッチ $\theta$ が0.12mm程度まで加工が可能となるが、更に厚さW1のとり方次第ではインナーリード先端部ピッチ $\theta$ は更に良いピッチまで可能となる。ちなみに、インナーリード先端部ピッチ $\theta$ を0.08mm、厚さ2.5mmで厚さW1を0.8mm程度が可能となる。

(0016) このようにエッティング加工にてリードフレームを作成するに、インナーリードの長さが大きい場合、加工工程でインナーリードのヨレが発生しない場合には、図9(a)に示す形状のリードフレームエッティング加工ではあるが、インナーリードの長さが長く、インナーリードにヨレが発生しやすい場合には、図9(c) (イ) に示すように、インナーリード先端部から厚さW1の1/2Bを抜け、インナーリード先端部に止む位置ににしてあらかじめ切削したものを用いて、ニッケル電極部には不必的な部分を1/2Bをプレス等により削除して図9(a)に示す形状を用う。尚、前述のように、図9(c) (イ) に示すものを切削し、図9(c) (ロ) に示す形状にする場合には、図9(c) (ロ) に示すように、各スリット部のため高さテープ1.6-0-(ポリイミドテープ)を接着する。図9(c) (ロ) の状態で、プレス等により厚さW1の1/2Bを切削するが、ニッケル電極部は、テープをかけた形状のまま、リードフレームに固定され、その位置が止まる位置にてリードフレームに止む部分を示すものである。

(0017) 本発明の特徴を述べに用いたリードフレームのインナーリード部の形状には、図13(イ) (a) に示すようになっており、ニッティングチップ131Aの厚さW1には逆手まで至るまでの厚さW2より厚さW1で大きくなっている。W1、W2 (mm) 0.08mm) ともこの部分の厚さW2がW1の厚さW2よりも大きくなっている。このようにインナーリード先端部の表面は広くなっているため、どちらか一方においても厚さW2 (図示せず) とインナーリード先端部131AとクライアントA、-1320Bによる面積 (ボンディング面) が大きいものとなっているが、本発明の特徴にはニッティングチップ (図13 (ロ) (a)) をボンディング面として用いて、厚さW1にニッティングチップ131Aによく接する面、131Aはリードフレームミリ版131A、1320Bにのっとせてある。ニッティングチップ面がアラビの長い面であるため、図13 (ロ) (a) の場合に、厚さW2 (ボンディング面) が止まらぬ、図13 (ハ) に示すように示す加工方法にて加工されたリードフレームのインナーリード先端部131Aと厚さW2 (図示せず) との面積 (ボンディング面) を示すものであるが、この場合インナーリード先端部131A

の表面に厚さW2ではあるが、この部分の面積を示すと非常に大きい。また表面ともリードフレーム面であります。表面 (ボンディング面) には厚さW2、厚さW2のチップ面より厚さW2 (ニッティング面) によりインナーリード先端部を肉化した面上に1331Dを加工したものの、ニッケル電極部 (S示す) との面積 (ボンディング面) を示したものであるが、この面積にプレス面がSに示すように二重になつていて、このためどちらの面を用いてもS (ボンディング面) しても、図11 (ニ) (a) (b) に示すようにS (ボンディング面) の間に厚さW2がなく品切れにしやすくなる場合が多い。尚、1331Aの面にニッティング面である。(0018) 次に又本発明の取扱止型ニッケル電極の本発明を示す。図3 (a) ~図3 (c) に、それぞれ、又本発明の取扱止型ニッケル電極の本発明の構造図である。図3 (a) に示す又本発明のニッケル電極の本発明には、又本発明のニッケル電極とは、ダイパッド135の位置が異なるもので、ダイパッド135が位置に固定してある。ダイパッド135が位置に固定してあることにより、又本発明に比べ、他の取扱止が取れている。図3 (b) に示す又本発明のニッケル電極は、ダイパッド135が位置に固定されていいるものであって、又本発明に比べて他の取扱止が取れている。又本発明に図3 (a) に示す又本発明とは、ニッケルの厚さ1.0mmがなり、ワイヤボンディング面をリードフレームの裏面に面していいる。図3 (c) (ロ) (a) (b) に示す又本発明には、ニッケル電極131に、図3 (a) に示す又本発明、図3 (b) に示す又本発明において、ニッケルの厚さからなるコテ板を抜けず、又本発明の面を底面又本発明として用いていいる。尚、厚さW2を底面又本発明として用いていいる。(0019) 本発明の取扱止型ニッケル電極を示す。図4 (a) に示す又本発明の取扱止型ニッケル電極は、図4 (b) (c) に示す又本発明の取扱止型ニッケル電極である。尚、又本発明の取扱止型ニッケル電極の取扱止は、二重じとなる為、図4 (b) に示す又本発明の取扱止は、210はニッケル面、211は又本発明 (ハンド) 、220はワイヤ、230はリードフレーム、231はシングルリード、232は又本発明 (ハンド) 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例にウイナ220により、インテーリード231の端子231へ0と並んでいる。スマートの端子、スイッチ部には0と並んで、スマート200と並んで、その端子部には、モード233の端子部に並んでいたコネクタ部からうなう端子部233へを介してプリント基板へ接続されることにより行かれる。

(0020) また、支承部の2のニップル部には、図10 (a)、10 (b) に示す、ダイバードを用たない、エンジングにより丸孔加工されたリードフレーム230へを用いたもので、その直径万円に支承部1とは同じ大きさであるが、三なき底に、支承部1のときにはニップル部モインテーリードに固定したはずでワイヤボンディングを行い、右端が止しているのにかし、支承部2の場合は、半径は支承210モインテーリード231とともに~~支承部~~テープ270上に固定したので、ワイヤボンディングを行ない、右端が止しているのである。左端は、~~支承部~~のプレスによる半径部分の端子コテの底面は、~~支承部~~1と同様である。図10 (a) に示すリードフレーム230へをはるには、図9 (a) に示すリードフレーム230へをはたすと反対にしてある。これらは、~~支承部~~270に示すエンジングニニ2へたすのものをめあし、図10 (a) に示す形にしてある。この時、図10 (c) (c) に示すように、まず、~~支承部~~のため~~支承部~~260 (ポリイミドテニス) を用ひ、

(0.0.2.1) 図5 (a) ~ 図5 (c) に、元気外2のニ  
ヌヌヌヌの元気外ニヌヌヌヌの断面図である。図5  
(a) に示す支流側ニヌヌヌヌに、ニヌヌヌヌの内壁が  
図5 (a) で、内壁を下す面を下側にしていう。  
おこじフライヤポンディング壁モリードフレームの内1壁  
に沿って、内1壁でヌヌヌヌのヌヌヌヌと見なす。  
(b)、図5 (c) に示す元気外ニヌヌヌヌに、それ  
ハ元気外2のニヌヌヌヌ。図5 (a) に示す元気外のニ  
ヌヌヌヌにおいて、ニヌヌヌのニヌヌヌからなる内壁を内1  
壁、内1壁の壁を内1壁として用いていうのである。  
然しながら、内1壁の内1壁の内1壁の内1壁  
に取出している。チヌヌヌヌの内1壁のチヌヌヌヌ  
いがはとなつていて、

（0.0.2.2）次いで、天井内にのみが見出される事  
を述べる。図6（a）に天井内にのみが見出される  
点の詳細であり、図6（b）に図6（a）のAS-A  
6におけるインテリード部の断面図である。図6（c）は  
図6（a）のSS-B6におけるエチビヨの断面図であ  
る。然し、天井内にのみが見出されるのは、天井内にのみが  
見じとなう。図6（d）に示した、図6（e）300mmより  
天井、310にモルタル、312にパンプ、313に  
リードフレーム、314にインテリード、331A、  
331Bにスリット、331A6にスリット、331A7にスリット  
331A8にスリット、331Bにスリット、331B8にス  
リット、331B9にスリット、331Sに上部板、340に

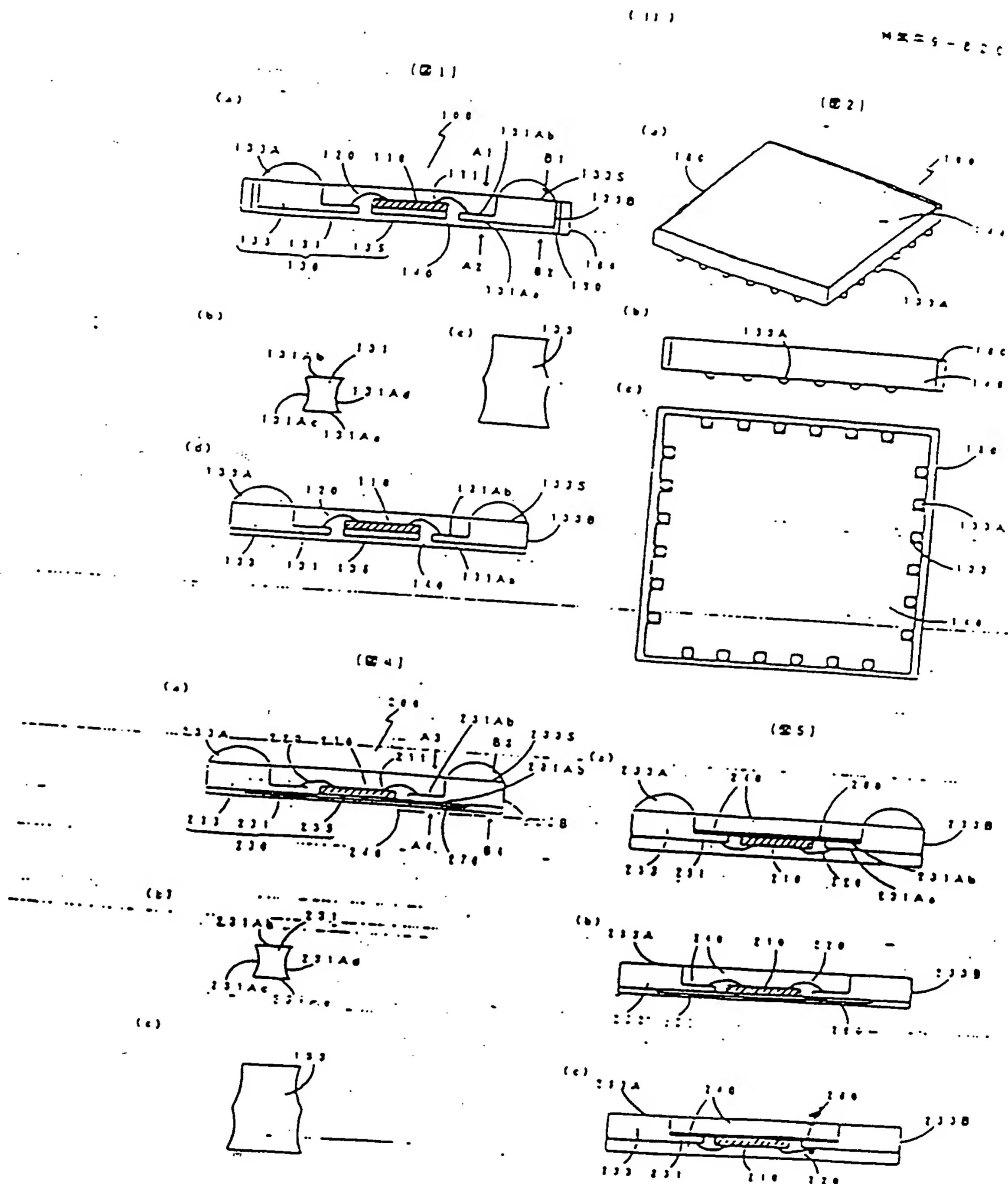
(0022) 本局のニコニコ便に、本局のニコニコ便の当さとに至り、区12に示すニシチングに上  
シテニコニコ便にビスレニムも用いたものである  
が、ニコニコ便の日本万葉には同じ工法である。  
是なる点に、本局のニコニコ便の当さには同じ工法である。  
ニモインナーリードに固定したままでワイヤボンディングを行い、本局止していふのに加し、本局内にニ  
コニコ便の当さには、ニコニコテ310モインナーリー  
ド331にパンプを介して固定して本局には及した  
事で本局止していふのである。本局止のアレ  
スによるニコニコ便の当さ、萬子の当さに、本局内1の  
ニコニコ便の当さと同じである。

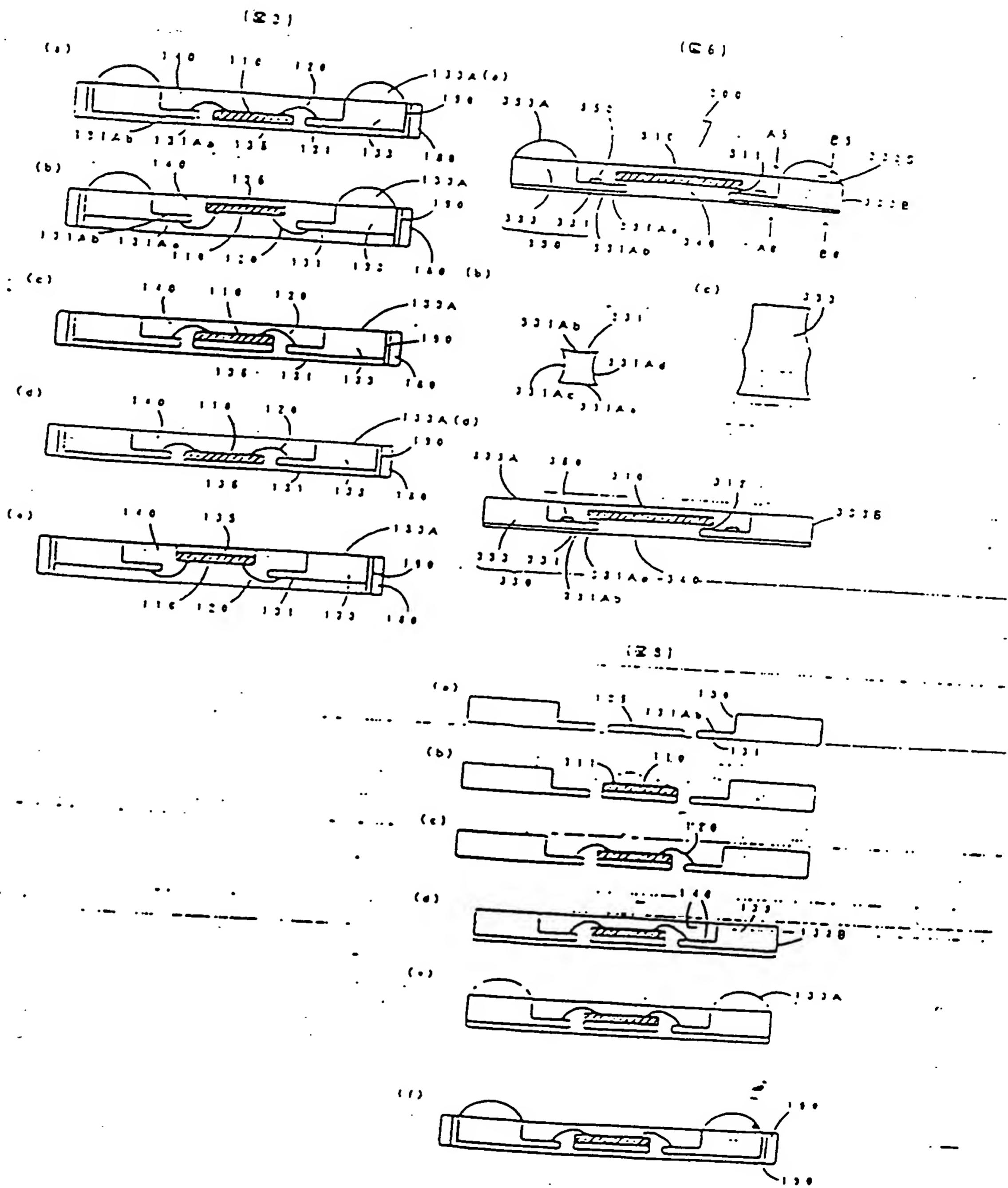
(0024) 区6 (a) に大阪府内の本拠地を有する支  
店の本拠地の所在地である。区6 (b) に大阪府  
内の本拠地に、大阪府の本拠地を有するにおいて、支  
店の本拠地からなる支店を立てて、支店の本拠地は支  
店として置いているものである。支店を置くして支  
店の本拠地の本拠地を別に置いている支店  
にて支店の本拠地のチニックがしない場合となっている。  
又にこの支店の本拠地の本拠地をばねて置くと上  
からチニックしない理由とてうこととしてある。  
(0025) おいて、大阪府の本拠地を有する支  
店に、支店 (a) に大阪府の本拠地を有する支  
店の本拠地であり、支店 (b) に支店 (a) の本拠地  
におけるインテリード店の本拠地で、区6 (c) に  
6 (a) の67-98における支店の本拠地である  
。大阪府の本拠地を有する支店の本拠地には  
じとならぬ。区6 (d) に支店 (a) の本拠地  
。410に支店 (b) 、411に支店 (c) 、430に

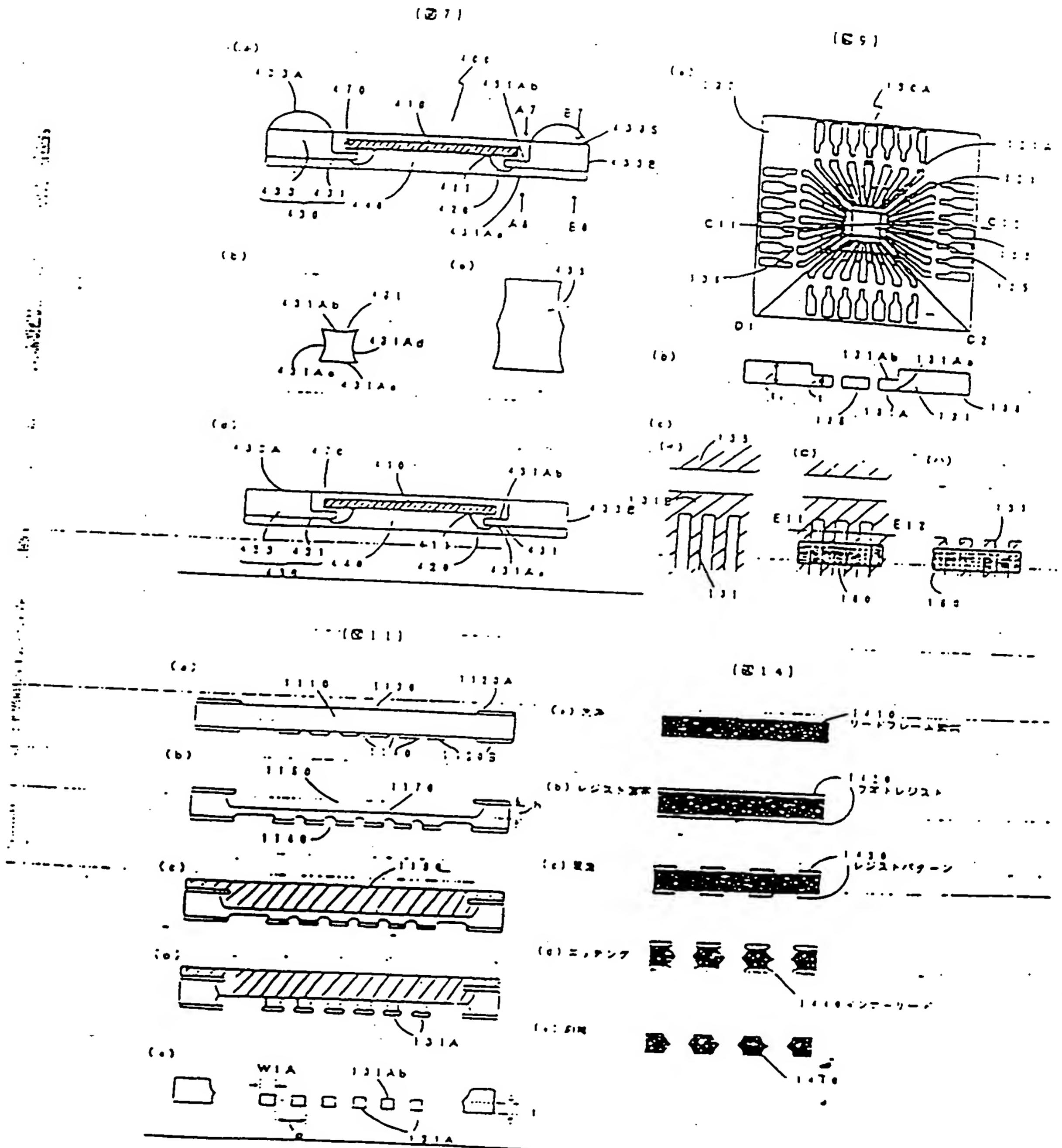


190	ードフレームニシキ
200	1331A8
260	イニシング面
260 使用テープ	1410
270	ードフレームニシキ
270 生地支尾テープ	1420
350	オトレジスト
350 使用テープ	1430
470	ジストバーン
470 生地支尾	1440
1110	ンターリード
1120A, 1120B ジストバーン	1510
1130	ードフレーム
1130 一の端ニシキ	1511
1140	イバッド
1150 二の端ニシキ	1512
1150 一の端ニシキ	1512A
1160	ンターリード元支尾
1160 二の端ニシキ	1513
1170	クターリード
1180 ンチング元支尾	1514
1320A, 1320C, 1320Q イテ	1515
1321B, 1321C, 1321D 1331B, 1331C, 1331D ンターリード元支尾	レーム面 (A面) 1520 スリッテ 1521 面 (バッド) 1530
1331A2	1540 止用面

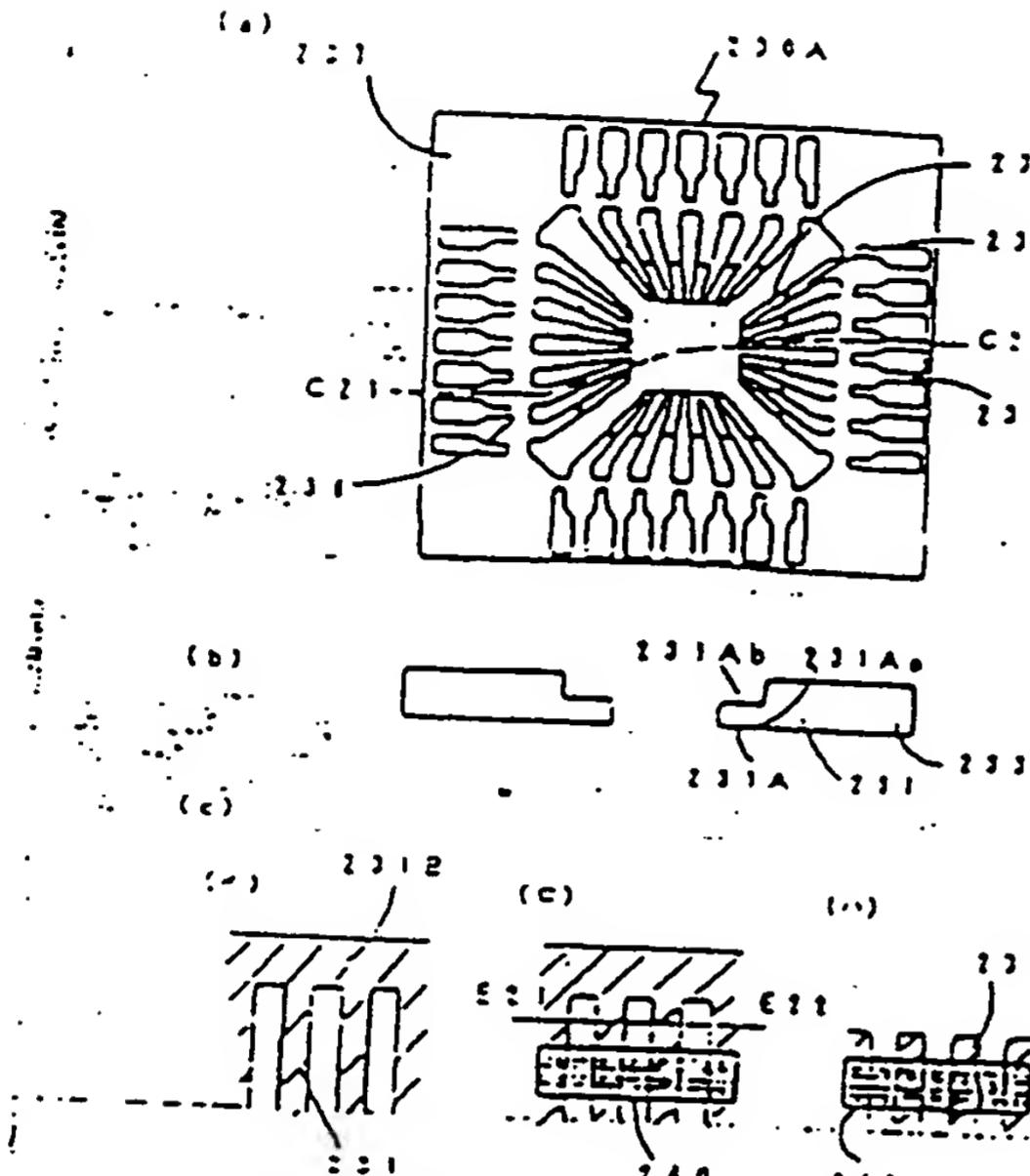
MAX 9 - 82005



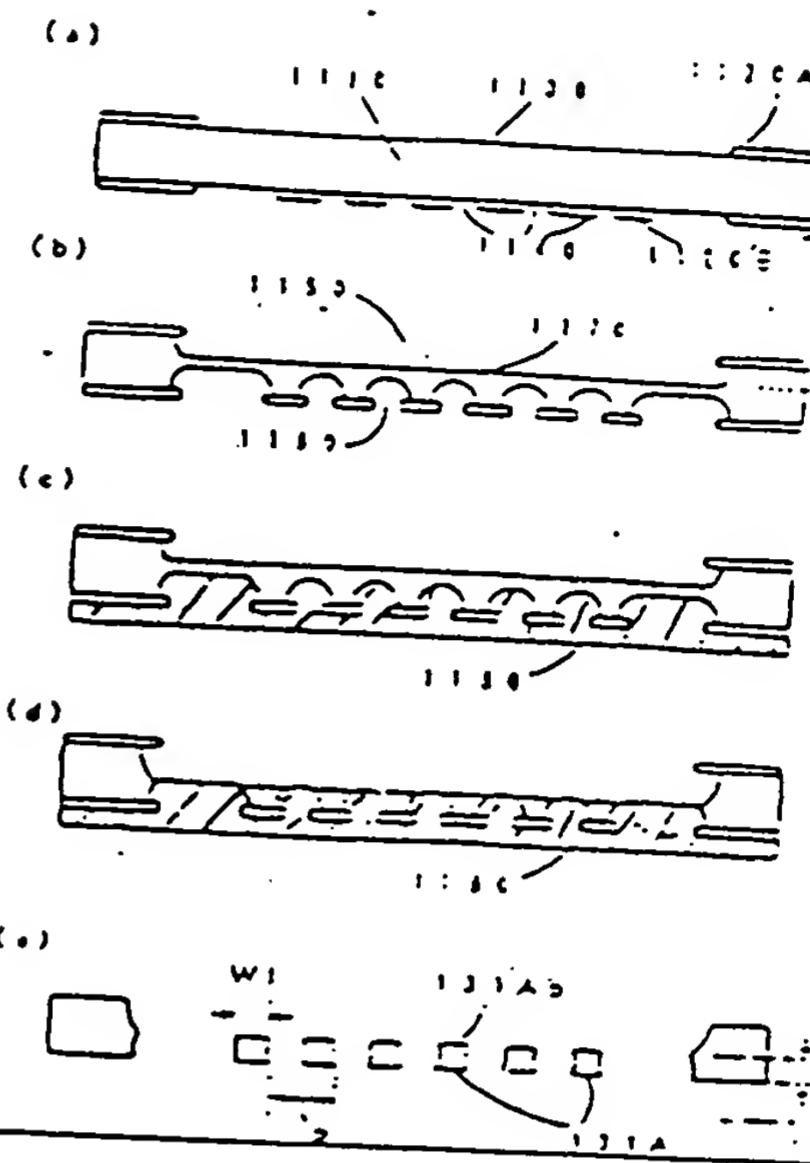




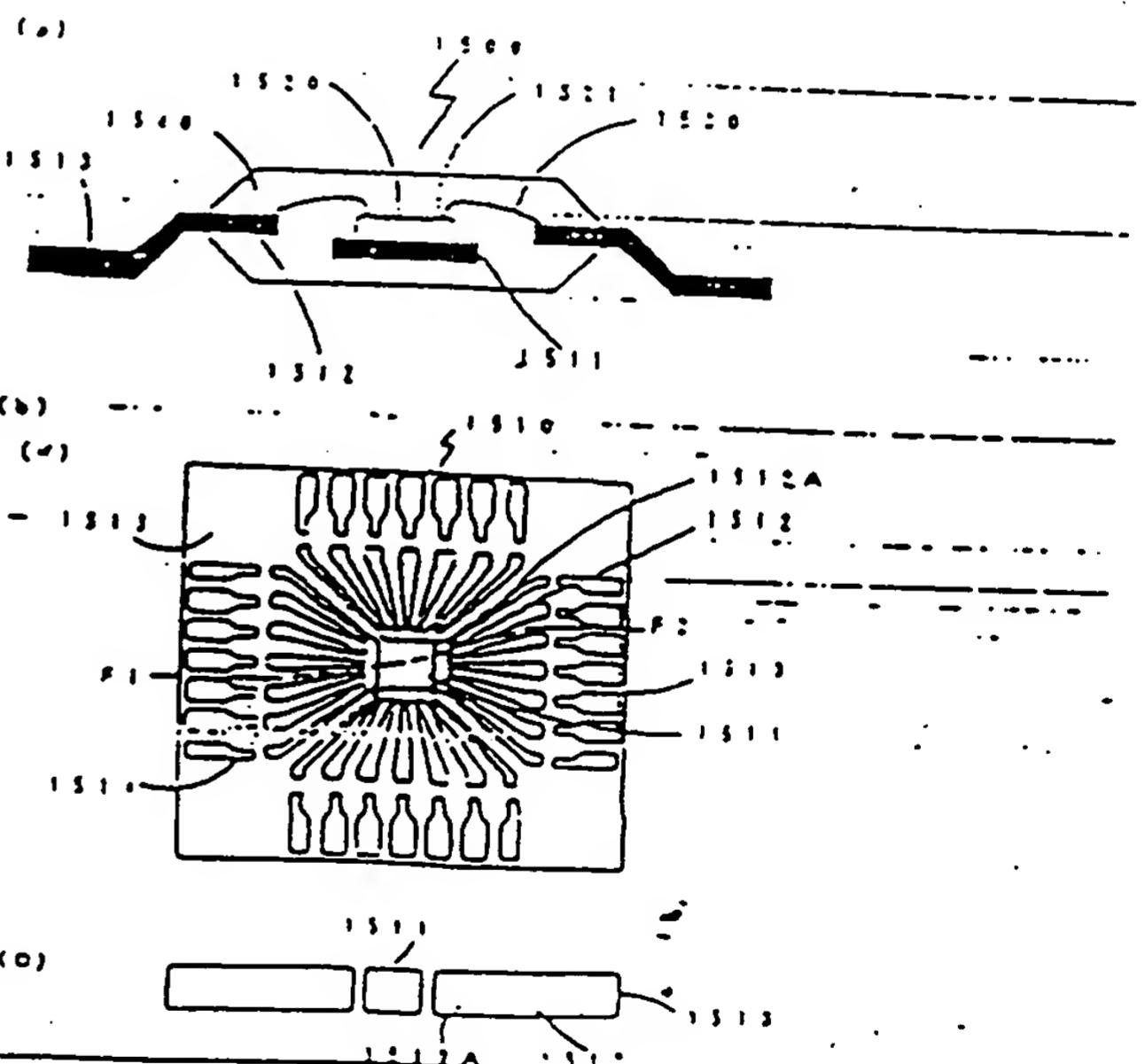
(610)



12:21



१४५



(Σ : 2)

